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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/607,949	06/27/2003	Howard Levy	004-8850	3054

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EXAMINER
TAN, VIBOL

ART UNIT	PAPER NUMBER
2819	

DATE MAILED: 03/24/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

H.A

Office Action Summary	Application No.	Applicant(s)	
	10/607,949	LEVY ET AL.	
	Examiner	Art Unit	
	Vibol Tan	2819	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 March 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-3,5-23,25-27 and 30-36* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *30-34* is/are allowed.

6)☒ Claim(s) *1-3, 5-7, 9, 13, 19-23, 25-27, 35 and 36* is/are rejected.

7)☒ Claim(s) *8,10-12 and 14-18* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Applicant's request for reconsideration of the finality of the rejection of the last Office action is persuasive and, therefore, the finality of that action is withdrawn. In view of newly cited reference, however, a new rejection is set forth below.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 1-3, 5-7, 9, 13, 19, 20, 23, 25-27, 35 and 36 are rejected under 35 U.S.C. 102(e) as being anticipated by Kursun et al. (US 2004/0008056 A1).

In claim 1, Kursun et al. teaches all claimed features in Fig. 12, a keeper circuit for a dynamic node (128) of a circuit, wherein the effective strength (keeper gate drive; [0077], line 2) of the keeper circuit (P2) operating on the dynamic node is reduced from a non-zero strength level (V_{DD}) to a second non-zero strength level ($|V_{tp}|$, assuming $|V_{tp}|$ is than or equal to V_{th}; [0079], line 9) during an interval (an interval between V_{DD} and $|V_{tp}|$) in which at least one path in an evaluation circuit (Pulldown Network) is sensitive to a keeper device (P2).

In claims 2-3, Kursun et al. further teaches the circuit of claim 1, wherein the sensitivity of the at least one path includes output of an incorrect value of the evaluation

circuit output (noise); wherein a response to the sensitivity is otherwise a reduced speed of the evaluation circuit output (improve the delay; [0077], line 3).

In claim 5, Kursun et al. teaches all claimed features in Fig. 12, a circuit comprising: a dynamic node (128); an evaluation circuit (Pulldown network) coupled to the dynamic node; a keeper circuit (P2, P3, N6) coupled to the dynamic node (128) wherein the keeper circuit has a first non-zero strength (V_{DD}) during a first interval and a second non-zero strength ($|V_{tp}|$, assuming $|V_{tp}|$ is than or equal to V_{th}; [0079], line 9) during a second interval, the first non-zero strength being substantially greater than the second non-zero strength ($V_{DD} > |V_{tp}|$).

In claims 6 and 7, Kursun et al. further teaches the circuit of claim 5, wherein the keeper circuit (P2, P3, N6) latches an output (output at node 128) of the circuit; and wherein the keeper circuit includes a first keeper device (P2).

In claim 9, Kursun et al. further teaches the circuit of claim 5, wherein the keeper circuit includes a week keeper device (P2).

In claim 13, Kursun et al. further teaches the circuit of claim 5, comprising: a clock node (clock); a precharge device (P1) couple to the clock node and the dynamic node; and a discharge device (Foot) coupled to the clock node and the evaluation circuit.

In claim 19, Kursun et al. further teaches the circuit of claim 5, wherein the dynamic node (128) is precharged high (V_{DD}).

In claim 20, Kursun et al. further teaches the circuit of claim 19, wherein the evaluation circuit is n-logic (1114 in Fig. 14).

In claim 23, Kursun et al. teaches all claimed features in Fig. 12, a method for evaluating a dynamic node, comprising: precharge a dynamic node (128); effectively disabling a first keeper device (when a logic level is low at a gate of P2) coupled to the dynamic node during an interval in which at least one path in an evaluation circuit is sensitive to a keeper device; evaluating an evaluation circuit (Pulldown Network); protecting the dynamic node from noise ([0077], line 4) during the interval; and effectively enabling (when the logic level is high at the gate of P2) the first keeper device.

Claims 25 and 26 correspond to detailed circuitry already discussed similarly with regard to claim 1.

Claim 27 corresponds to detailed circuitry already discussed similarly with regard to claim 23.

In claim 35, Kursun et al. further teaches the circuit of claim 23, wherein the dynamic node (128) is protected by at least a weak keeper (P2).

Claim 36 corresponds to detailed circuitry already discussed similarly with regard to claim 35.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claims 21 and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Kursun et al. in view of Karnik et al. (U. S. PAT. 6,366,132).

In claim 21, Kursun et al. teaches all claimed features the circuit of claim 5; with the exception of teaching wherein the dynamic node is precharged low. However, Karnik et al. teaches in Fig. 9, the dynamic node (N50) is precharged low (when T44 is closed).

Therefore; it would have been obvious to one ordinary skill in the art at the time of the invention was made to precharge the dynamic node of Kursun's circuit to low level or ground, in order to provide another version of Kursun's circuit.

In claim 22, Kursun et al. teaches all claimed features the circuit of claim 5; with the exception of teaching wherein the evaluation circuit is p-logic. However, Karnik et al. teaches in Fig. 9, the evaluation circuit (94) is p-logic (P-stack).

Therefore; it would have been obvious to one ordinary skill in the art at the time of the invention was made to precharge the dynamic node of Kursun's circuit to low level or ground, in order to provide another version of Kursun's circuit.

6. Claims 8, 10-12 and 14-18 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

7. Claims 30-34 appear to comprise allowable features.

Response to Arguments

8. Applicant's arguments with respect to claims 1, 5, 23, 25 and 27 have been considered but are moot in view of the new ground(s) of rejection.

The newly cited reference of Kursun et al. anticipates claims 1-3, 5-7, 9, 13, 19, 20, 23, 25-27, 35 and 36 whereas the combination of Kursun et al. and Karnik et al. teaches claims 21 and 22, as discussed in details above.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Vibol Tan whose telephone number is (571) 272-1811. The examiner can normally be reached on Monday-Friday (7:00 AM-4:30 PM).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mike J. Tokar can be reached on (571) 272-1812. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

VIBOL TAN
PRIMARY EXAMINER